IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 10/729,751 Applicant(s): Bonaccio et al.

Filed.: December 4, 2003 Art Unit: 2115

Dkt. No.: BUR9-2003-0099 Examiner: Bae, Ji H

Title: **DIGITIAL RELIABILITY MODEL HAVING AUTOMATIC REPAIR AND NOTIFICATION CAPABILITY**

Honorable Commissioner for Patents
P. O. Box 1450
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REQUEST FOR RECONSIDERATION

This Request for Reconsideration is being filed in response to the Office Action mailed on March 30, 2006.

In the Claims:

Please amend claims 1-3, 7-8, 10, 12-16, and 21. The claims are as follows:

1. (Currently Amended) An integrated circuit, comprising:

a pulse generator ~~adapted to generate~~ for generating a pulsed signal;

a cycle counter ~~adapted to count~~ for counting cycles of said pulsed signal;

one or more repairable circuit elements; and

a repair processor ~~adapted to repair~~ for repairing a repairable circuit element of said one or more circuit elements when said cycle counter reaches a pre-determined cycle count.

2. (Currently Amended) The integrated circuit of claim 1, wherein said repair processor[[,]] ~~replaces~~ is adapted to permanently disable said repairable element and replace said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

3. (Currently Amended) The integrated circuit [[if]] of claim 1, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

4. (Currently Amended) The integrated circuit of claim 1, further including a memory circuit ~~adapted to store~~ for storing a cycle count of the number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

5. (Original) The integrated circuit of claim 1, wherein:

said cycle counter is adapted to generate a trigger signal when said predetermined cycle count is reached; and

said repair processor is adapted to receive said trigger signal and affect a repair of said repairable circuit element when said trigger signal is received.

6. (Original) The integrated circuit of claim 5, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

7. (Currently Amended) The integrated circuit of claim 1, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device[[s]], a transistor, a diode, a resistor[[s]], capacitor, an inductor and a wire.

8. (Currently Amended) The integrated circuit of claim 1, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor ~~programs~~ is adapted to program a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

9. (Original) The integrated circuit of claim 1, further including a fuse bank for storing information used to implement a repair of said repairable circuit element.

10. (Currently Amended) The integrated circuit of claim 1, wherein [[in]] said repair processor is adapted to perform multiple repairs by repairing previously repaired repairable circuit elements.

11. (Original) The integrated circuit of claim 1, further including:

a redundant cycle counter; and

wherein said repair processor is adapted to replace said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

12. (Currently Amended) A method of preemptively repairing an integrated circuit, comprising:

(a) providing a pulse generated adapted to generate a pulsed signal;

(b) providing a cycle counter adapted to count cycles of said pulsed signal;

(c) providing one or more repairable circuit elements; ~~and~~

(d) providing a repair processor adapted to repair a repairable circuit element of said one or more repairable circuit elements when said cycle counter reaches a pre-determined cycle count; and

(e) repairing said repairable circuit element when said cycle counter reaches said pre-determined cycle count.

13. (Currently Amended) The method of claim 12, wherein said step [[(d)]] (e) includes permanently disabling said repairable element and replacing said ~~one or more~~ repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

14. (Currently Amended) The method [[if]] of claim 12, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

15. (Currently Amended) The method of claim 12, further including a memory circuit ~~adapted to store~~ for storing a cycle count of a number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

16. (Currently Amended) The method of claim 12, ~~wherein~~ further including:

said cycle counter ~~is adapted to generate~~ generating a trigger signal when said predetermined cycle count is reached; and

said repair processor is ~~adapted to receive~~ receiving said trigger signal and ~~affect a repair of~~ repairing said repairable circuit element when said trigger signal is received.

17. (Original) The method of claim 16, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

18. (Original) The method of claim 12, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

19. (Original) The method of claim 12, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor programs a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

20. (Original) The method of claim 12, further including providing a fuse bank for storing information used to implement a repair of said repairable circuit element.

21. (Currently Amended) The method of claim 12, further including ~~wherein in~~ said repair processor ~~is adapted to perform~~ performing multiple repairs by repairing previously repaired repairable circuit elements.

22. (Original) The method of claim 12, further including:

providing a redundant cycle counter; and

said repair processor automatically replacing said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

23. (Withdrawn) A method for designing a repairable integrated circuit, comprising:

generating an integrated circuit design from a design library of circuit elements;

simulating said integrated circuit design and generating a switching report for circuit elements of said integrated circuit design;

selecting a circuit element responsive to a pulsed signal of said integrated circuit design based on said switching report;

selecting a repairable circuit element from said design library, said repairable circuit element having the same function as said selected circuit element and allowing multiple connection paths; and

inserting said selected repairable circuit element, a cycle counter adapted to count cycles of said pulsed signal and repair processor adapted to repair said repairable circuit element when said cycle counter reaches a pre-determined value into said integrated circuit design.

24. (Withdrawn) The method of claim 23, wherein said switching report indicates a number of state toggles of each selected circuit element performed during said simulation.

25. (Withdrawn) The method of claim 23, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistors, a diode, a resistor, a capacitor, an inductors and a wire.

26. (Withdrawn) The method of claim 23, wherein said repairable circuit element is implemented in a field programmable gate array having spare gates and said repair processor includes a circuit for programming said field programmable array to use programmed spare gates in place of the gates originally programmed to implement said repairable circuit element.

27. (Withdrawn) A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method

for a method for designing a repairable integrated circuit, said method comprising the computer implemented steps of:

generating an integrated circuit design from a design library of circuit elements;

simulating said integrated circuit design and generating a switching report for circuit elements of said integrated circuit design;

selecting a circuit element responsive to a pulsed signal of said integrated circuit design based on said switching report;

selecting a repairable circuit element from said design library, said repairable circuit element having the same function as said selected circuit element and allowing multiple connection paths; and

inserting said selected repairable circuit element, a cycle counter adapted to count cycles of said pulsed signal and repair processor adapted to repair said repairable circuit element when said cycle counter reaches a pre-determined value into said integrated circuit design.

28. (Withdrawn) The system of claim 27, wherein said switching report indicates a number of state toggles of said circuit element performed during said simulation.

29. (Withdrawn) The system of claim 27, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

30. (Withdrawn) The method of claim 27, wherein said repairable circuit element is implemented in a field programmable gate array having spare gates and said repair processor includes a circuit for programming said field programmable array to use programmed spare gates in place of the gates originally programmed to implement said repairable circuit element.

REMARKS

The Examiner has required affirmation of a telephone election. In response, Applicants affirm that in a telephone conversation on March 22, 2006 between Examiner Ji H. Bae and Applicants representative William Steinberg, Applicants representative elected claims 1-22 without traverse. In view of the Examiner's earlier restriction requirement, Applicants retain the right to present un-elected claims 23-30 in a divisional application

The Examiner has objected to claims 3, 7, 10, 12 and 14 because of typographic errors. In response, Applicants have amended claims 3, 7, 10, 12 and 14 to correct the typographic errors.

The Examiner rejected claims 12-20 under 35 U.S.C. 112 (second paragraph) as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

The Examiner rejected claim 12 under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner rejected claims 1-5, 10, 12-16, and 21 under 35 U.S.C. §102(b) as being unpatentable over Evans et al. (US Patent 6,425,092).

The Examiner rejected claims 6-9, 11, 17-20, and 22 under 35 U.S.C. 103(a) as being unpatentable over Nogami et al. (US Patent 5,459,342 in view of Evans (6,425,092).

Applicants respectfully traverse the §101, §112, §102(b) and §103(a) rejections with the following arguments.

35 USC § 101

The Examiner rejected claim 12 under 35 U.S.C §101, stating "Regarding claim 12, applicant has recited a 'method of preemptively repairing an integrated circuit'. However, applicant has only listed steps for providing the various components in the circuit that are needed to provide the repairing feature. Applicant has not recited any steps that actually accomplish the repairing step. Therefore, applicant's method does not achieve the claimed objective of preemptively repairing an integrated circuit. As such, applicant's claimed method is non-statutory because it does not provide a useful, concrete, or tangible result."

In response, Applicants have amended claim 12 to include an actual repairing step and now believe claim 12 complies with the requirements of 35 U.S.C §101.

35 USC § 112

The Examiner rejected claims 2-12 under 35 U.S.C §112, (second paragraph) stating "Regarding claim 12, the typographical error in line 2 renders the scope of the claim indefinite, as it is unclear to the examiner what is being claimed. Claims 13-22 are rejected by virtue of their dependency."

In response, Applicants have amended claim 12 to correct the typographic error and believe that claim 12 is now definite under 35 U.S.C §112, (second paragraph). Since claims 13-22 depend from claim 12, Applicants believe that claims 13-22 are now definite under 35 U.S.C §112, (second paragraph).

35 USC § 102

As to claims 1 and 12, the Examiner states that "Evans teaches an integrated circuit comprising: a pulse generator adapted to generate a pulsed signal; a cycle counter adapted to count cycles of said pulsed signal [Fig. 3, interval timer 60];one or more repairable circuit elements [chip section 1 and chip section 2]; and a repair processor adapted to repair a repairable circuit element when said cycle counter reaches a pre-determined cycle count [control logic and I/O switching logic]. The interval timer of Evans counts to a predetermined time period, after which it issues a signal to the control logic to switch between chip sections 1 and 2 [col. 4, lines 10-22]. The chip sections are redundant, and are used to substitute for one another when there is a risk of overheating, determined in this case by a predetermined interval timer value. Since the interval timer is used to count to a predetermined time value, it must inherently count cycles of a pulsed signal (e.g. a clock)."

Applicants contend that claims 1 and 12 are not anticipated by Evans et al. because Evans et al. does not teach each and every feature of claims 1 and 12. For example Evans et al. does not teach "a repair processor adapted to repair a repairable circuit." Applicants respectfully point out that Evans et al. does not **repair** either of chip sections 1 or 2 but temporarily **replaces** chip section 1 with chip section 2 and then temporarily replaces chip section 2 with chip section 1 and so on. Applicants point out that swapping one circuit element for another is not affecting a repair of the replaced circuit element because nothing has been actually done to the swapped out circuit element and it is reused with out any changes to it of any sort. Swapping out a circuit element might be considered a repair of the integrated circuit chip, but can not be considered a repair of the circuit element itself. Further, chip elements 1 and 2 of Evans et al. are not taught as being

repairable, just identical. There is no teaching in Evans et al. that any elements of chip sections 1 or 2 are repairable.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 and 12 are not unpatentable over Evans et al. and are in condition for allowance. Since claims 2-11 depend from claim 1 and claims 13-22 depend from claim 12, Applicants respectfully maintain that claims 2-11 and 13-22 are likewise in condition for allowance.

As to claims 2 and 13, the Examiner states that "Evans teaches that the repair processor replaces said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element."

Applicants contend that claims 2 and 13, as amended, are not anticipated by Evans et al. because Evans et al. does not teach each and every feature of claim 2 and 13. For example Evans et al. does not teach "permanently disabling said repairable element" Applicants respectfully point out that Evans et al. reuses chip sections 1 and 2 while Applicants repairable circuit is not used again.

Based on the preceding arguments, Applicants respectfully maintain that claims 2 and 13 are not unpatentable over Evans et al. and is in condition for allowance.

As to claims 4 and 15, the Examiner states that "Evans teaches a memory circuit adapted to store a cycle count of the number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit [sequential switching, initial offsets after reset, col. 4; lines 23-33]."

Applicants respectfully point out that the relevant teaching by Evans in col. 4, lines 23-33 is "Reset or initialization would require initial offsets in counters for each section in the control logic" but does not teach how to accomplish this. It is not inherent that counts be stored in memory. For example, the offset could be calculated using an algorithm.

Based on the preceding arguments, Applicants respectfully maintain that claims 4 and 15 are not unpatentable over Evans et al. and are in condition for allowance.

As to claims 10 and 21, the Examiner states that "Evans teaches said repair processor is adapted to perform multiple repairs by repairing previously repaired repairable circuit elements."

Applicants respectfully point out that Evans does not teach repairing a previously repaired circuit, only swapping circuits in and out, none of which have been repaired. Applicants believe the arguments provided *supra* with respect to claims 1 and 12 are applicable to claims 10 and 21.

Based on the preceding arguments, Applicants respectfully maintain that claims 10 and 21 are not unpatentable over Evans et al. and are in condition for allowance.

35 USC § 103 Rejections

As to claims 6-9, 11, 17-20, and 22, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claims 1 and 12 that claims 1 and 12 are allowable, since claims 6-9, 11, depend from claim 1 and claims 17-20, and 22 depend from claim 12, Applicants respectfully maintain that claims 6-9, 11, 17-20, and 22 are not unpatentable over Nogami in view of Evans and are in condition for allowance.

The examiner has rejected claims 6-9, 11, 17-20, and 22 over Nogami in view of Evans, indicating Nogami is the primary reference. Applicants point out that Nogami teaches only an FPGA and programming unused portions of the FPGA with circuit functions previously programmed in defective sections of the FPGA.

As to claims 6 and 7, Applicants do not understand which reference the Examiner is quoting for the claimed elements (trigger signal, current cycle count, any kind of circuit element). Applicants are unable to respond to the Examiners rejection of claims 6 and 7 and request clarification.

As to claim 8, Applicants point out that the control logic 30 and switching logic 44 of Evans et al. can not program an FPGA, as they can not send out the proper signals. Control logic 30 only sends out enable signal to chip sections 1 and 2 to turn them on and off and a set signal to switching logic and enable/disable signals to I/O functions 40 to disconnect signals going in and out of chip sections 1 and 2.

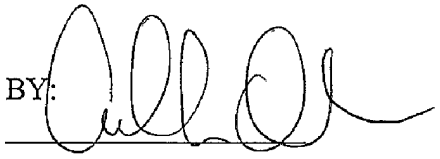
As to claim 11, First there is absolutely no teaching in either Nogami or Evans about a second (redundant cycle counter). Second, the Examiners has not provided a reason to combine references. The examiners statement "it would have been obvious to one of ordinary skill in the art to provide a redundant cycle counter and replace the cycle counter after a fixed count" does not give a reason for talking the action, just the action itself. The Examiners has therefore not established a *prima facie* case of obviousness. Third, the Examiners statement of how to implement a second cycle counter (using the FPGA of Nogami) does not appear in either Nogami or Evans and has impermissibly been supplied by the Examiner.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Respectfully submitted,
FOR: Bonaccio et al.

Dated: 6-19-2006

BY: 

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